REMARKS

In response to the Office action, applicant has added a limitation into claims 1-2, 4-10, 11, and 21, whereby the claimed thin film transistor is "single-gated."

Claim Rejections under 35 U.S.C. 103

Claims 1-2, 4-6, 8-10 and 21 are rejected under 35 U.S.C. 103(a) as being anticipated by Denton et al. ("Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI islands with an Isolated Buried Polysilicon Backgate," IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511) in view of Hiramatsu et al. (U.S. Pat. 5,311,040).

Examiner states that "Denton (FIG. 1) discloses a thin film transistor, comprising: a substrate; [and] a gate electrode (polysilicon bottom gate) disposed in the substrate..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode."

In response to the rejection, applicant has, inter alia, amended independent claims 1 and 21. Applicant asserts that the rejected claims are now patentable, as follows:

Amended claim 1 recites in pertinent part "a **single-gated** thin film transistor, comprising: a substrate; **a gate electrode disposed in the substrate, the gate electrode being made of metallic material.**"

Firstly, the thin film transistor disclosed by Denton comprises a

bottom gate disposed in a substrate and made of polysilicon, whereas the single-gated thin film transistor of amended claim 1 comprises **a gate electrode disposed in a substrate and made of metallic material**. Secondly, the thin film transistor disclosed by Denton further comprises a top gate. That is, the thin film transistor disclosed by Denton is a dual-gated thin film transistor, whereas the thin film transistor of amended claim 1 is a single-gated thin film transistor. These differences indicate that Denton does not teach a single-gated thin film transistor comprising all the limitations recited in amended claim 1.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a substrate**.

Therefore, there is no motivation or suggestion in either Denton or Hiramatsu that the reference be combined with the other in such a way as to provide a single-gated thin film transistor comprising all the limitations recited in amended claim 1. Moreover, the single-gated thin film transistor of amended claim 1 produces new and unexpected results. That is, **the gate electrode made of metallic material is deposited in the substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the single-gated thin film transistor of amended claim 1 can efficiently reduce an RC (resistance-capacitance) delay of a scanning signal.

Accordingly, amended claim 1 is submitted to be unobvious and patentable over Denton in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of

amended claim 1 are respectfully requested.

Claims 2, 4-6 and 8-10 depend directly and indirectly from independent amended claim 1, and therefore should also be allowable.

For similar reasons to those asserted above in relation to amended claim 1, it is submitted that Denton combined with Hiramatsu does not disclose, teach or suggest all the limitations of the single-gated thin film transistor of the display device recited in amended claim 21.

Accordingly, amended claim 21 is submitted to be unobvious and patentable over Denton in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of amended claim 21 are respectfully requested.

Claims 1-2, 4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (U.S. Pat. 6,423,578) in view of Hiramatsu et al. (U.S. Pat. 5,311,040).

Examiner states that "Maeda (FIG. 9) discloses a thin film transistor comprising: a substrate 50a, [and] a gate electrode 41 disposed in the substrate 50a..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode."

Amended claim 1 recites in pertinent part a **single-gated** thin film transistor, comprising: a substrate; **a gate electrode made of metallic material disposed in the substrate**; and a gate insulation layer disposed

on the substrate and the gate electrode.

Applicant asserts that the rejected claims are now patentable, as follows:

As regards claim 1, Maeda (FIG. 9) discloses that a thin film transistor comprises a first support substrate 10, a lower gate electrode 41 positioned on the side of the first support substrate 10, [and] an insulator 50a (column 4, lines 21-23). However, the **single-gated** thin film transistor of amended claim 1 comprises **a gate electrode made of metallic material disposed in the substrate.** These differences indicate that Maeda does not teach a single-gated thin film transistor comprising all the limitations recited in amended claim 1.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a substrate**.

Therefore, there is no motivation or suggestion in either Maeda or Hiramatsu that the reference be combined with the other in such a way as to provide a single-gated thin film transistor comprising all the limitations recited in amended claim 1. Moreover, the single-gated thin film transistor of amended claim 1 produces new and unexpected results. That is, **the gate electrode made of metallic material is deposited in the substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that the single-gated thin film transistor of amended claim 1 can efficiently reduce an RC (resistance-capacitance) delay of a scanning signal.

Accordingly, amended claim 1 is submitted to be unobvious and patentable over Maeda in view of Hiramatsu under 35 U.S.C. 103(a). Reconsideration and withdrawal of the rejection and allowance of amended claim 1 are respectfully requested.

Claims 2, 4 and 6-7 depend directly from independent amended claim 1, and therefore should also be allowable.

Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denton et al. in view of Hiramatsu (U.S. Pat. 5,311,040) and further in view of Honda (U.S. Pat. 6,639,246).

Examiner states that Denton (FIG. 1) discloses, inter alia, a thin film transistor, comprising: a substrate; [and] a gate electrode (polysilicon bottom gate) disposed in the substrate..." Examiner further states that "Hiramatsu (FIG. 1) discloses a gate electrode 2, which is made of Ta or MoTa (column 3, lines 25-26) in order to increase conductivity of the semiconductor gate electrode." Examiner still further states that "Honda (FIG. 9) discloses a display device including a plurality of thin film transistors."

In response to the rejection, applicant has amended claim 11. Applicant asserts that the rejected claims are now patentable, as follows:

Amended claim 11 recites in pertinent part a display device including: a plurality of **single-gated** thin film transistors, each of the **single-gated** thin film transistors comprising a substrate; and **a gate electrode disposed in the substrate, the gate electrode being made of metallic material.**

Firstly, the thin film transistor disclosed by Denton comprises a bottom gate disposed in a substrate and made of polysilicon, whereas the **single-gated** thin film transistor of amended claim 11 comprises **a gate electrode disposed in a substrate and made of metallic material**. Secondly, the thin film transistor disclosed by Denton further comprises a top gate. That is, the thin film transistor disclosed by Denton is a dual-gated thin film transistor, whereas the thin film transistor of amended claim 11 is a single-gated thin film transistor. These differences indicate that Denton does not teach a single-gated thin film transistor comprising all the limitations recited in amended claim 11.

Further, Hiramatsu does not disclose a thin film transistor including **a gate electrode disposed in a substrate**.

Therefore, there is no motivation or suggestion in either Denton or Hiramatsu that the reference be combined with the other in such a way as to provide each of the single-gated thin film transistors of amended claim 11.

Even though Honda discloses a display device including a plurality of thin film transistors, Honda does not provide any additional teaching to the teachings of Denton or Hiramatsu which might lead one of ordinary skill in the art to provide each of the single-gated thin film transistors of amended claim 11.

Therefore, there is no motivation or suggestion in any of Denton, Hiramatsu or Honda that the reference be combined with the other in such a way as to provide a display device comprising all the limitations recited in amended claim 11.

Moreover, the display device of amended claim 11 produces new and unexpected results. That is, in each of the single-gated thin film transistors, **the gate electrode made of metallic material is deposited in the substrate**, and thus the thickness of the gate electrode can be changed by changing the depth of the substrate etched. As a result, it is easy to increase the thickness of the gate electrode to reduce its impedance, so that each of the single-gated thin film transistors of amended claim 11 can efficiently reduce an RC delay of a scanning signal.

Accordingly, amended claim 11 is submitted to be unobvious and patentable over Denton in view of Hiramatsu and further in view of Honda. Reconsideration and withdrawal of the rejection and allowance of amended claim 11 are respectfully requested.

Claim 12 depends from independent amended claim 11, and therefore should also be allowable.

In view of the foregoing, the present application as claimed in the pending claims is considered to be in a condition for allowance, and an action to such effect is earnestly solicited.

Respectfully submitted,
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